IN THE CLAIMS:

Please amend the claims as follows.

1-3. (Canceled).

4. (Previously presented) An instruction pipe control method comprising:

reading a call instruction from an instruction pipestage,

determining, with reference to other instructions read previously from the instruction pipestage, whether immediate processing of the call instruction would exceed a predetermined access rate of the instruction pipe to a return-stack buffer and,

stalling processing of the call instruction until sufficient time has expired to synchronize processing of the call instruction with the predetermined access rate.

5. (Original) The method of claim 4, further comprising, after the stalling terminates, storing a return address associated with the call instruction both locally and in a shared resource.

6. (Currently amended) The method of ~~claim 1~~claim 4, wherein the stalling stalls the instruction pipestage and all other instruction pipestages before it in the instruction pipe.

7. (Previously presented) An interface method for an instruction pipe that shares access to an external resource, comprising:

reading a call instruction from an instruction pipestage,

determining with reference to other instructions read previously from the instruction pipestage, whether immediate processing of the call instruction would cause the instruction pipe to exceed the instruction pipe's access allocation to the external resource,

if so, stalling the new instruction, and

after the stalling terminates, storing a return address associated with the call instruction both locally and in a shared resource.

8. (Canceled).

9. (Original) The method of claim 7, wherein the stalling stalls the instruction pipestage and all other instruction pipestages before it in the instruction pipe.

10. (Currently amended) A method for interfacing an instruction pipe with a return stack buffer having a predetermined round-trip communication latency period associated with a communication path therebetween, the method comprising:

reading a ~~new~~ return instruction from an instruction pipe stage,

determining, with reference to other instructions read previously from the instruction pipestage, whether a return address is available to the instruction pipe prior to expiration of the round-trip communication latency period with the return-stack buffer,

if not, stalling processing of the return instruction until the round-trip communication latency period expires.

11. (Currently amended) The method of claim 10, further comprising[[:]]

determining whether the new instruction requires access to ~~the~~ an external resource in excess of an access allocation for the instruction pipe, and

if so, stalling the ~~new~~ return instruction.

12. (Original) The method of claim 10, wherein the stalling stalls the instruction pipestage and all other instruction pipestages before it in the instruction pipe.

13-16. Canceled.

17. (Currently amended) Execution logic for a processor, comprising:

a first instruction pipe, comprising:

_____a first plurality of cascaded pipestages, and

a return stack buffer provided in communication with at least one of the first pipestages; and

a second instruction pipe, comprising:

a second plurality of cascaded pipestages, at least one of the second plurality of pipestages provided in communication with the return stack buffer, and

clock throttling logic coupled to the at least one second pipestage.

18. (Currently amended) The execution logic of claim 17, wherein the clock throttling logic comprises:

a state machine coupled to an output of the at least one pipestage from the second plurality of pipestages,

a clock control circuit having an input for a system clock signal and having an output for a modified clock signal, the output coupled to the at least one pipestage, the clock control circuit controlled by the state machine.

19. (Currently amended) The execution logic of claim 17, further comprising, in the first instruction pipe, second clock throttling logic that comprises:

a state machine coupled to an output of the at least one pipestage from the first plurality of pipestages,

a clock control circuit having an input for a system clock signal and having an output for a modified clock signal, the output coupled to the at least one pipestage, the clock control circuit controlled by the state machine.

20. (Original) The execution logic of claim 17, wherein additional instruction pipestages from either the first or the second instruction pipe are provided in communication with the return stack buffer, the additional instruction pipestages also provided with additional clock throttling logic.

21-22. (Canceled).

23. (Currently Amended) An instruction control method, comprising, responsive to a return instruction in a first pipestage of an instruction pipe:

determining whether a return address associated with the return instruction is stored in a register locally within the pipestage,

if so, passing the return address from the register to a next pipestage,

if not, retrieving the return address from a return stack buffer and stalling operation of all pipestages downstream of the first pipestage until the return address is received from the return stack buffer,

determining whether the pipestage processed a prior return instruction faster than a latency period for round trip communication between the pipestage and the return stack buffer,

if so, stalling the downstream pipestages until the period for processing a prior return instruction equals the round trip communication latency period.

24. (Canceled).

25. (Previously Presented) An instruction pipe, comprising:

a plurality of pipestages connected in cascade,

a pair of registers provided between first and second pipestages of the plurality,

a first of the registers to store a return address received from the first pipestage during receipt of a call instruction,

a second of the registers to store a return address received from a return stack buffer, and

a selector coupling the first and second registers to the second pipestage.

26. (Previously Presented) The instruction pipe of claim 25, further comprising a clock stopping circuit to control the second pipestage and pipestages downstream therefrom.